Williams Electronics, Inc.

Defender Servicing

ROM Board

Recap Sheet

The ARBEN Group

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This recap sheet covers troubleshooting the ROM board for the Defender Game. This sheet contains the most important points covered in the accompanying video tape. Use this recap sheet in conjunction with your Defender schematic diagrams to assist you later on in recalling information as you need it while performing your work.

The ROM board in the Defender game contains the main game programs.

The programs are selected on an as needed basis via an addressing system generated by the MPU on the CPU/Video board.

In addition the ROM board also contains the self-test diagnostic programs and Input/Output ports.

The input port is used by the system to check the status of the coin door switches.

The output port is used to control the on-board self-test indicator LEDs as well as the game play sounds that are produced by the sound board.

As was shown in the video, the ROM board is an integral part of the total Defender system. The video then took a closer look at the specific circuits that comprise the ROM board.

The ROM board includes the ROMs themselves, a Page Select circuit, Address Decoding circuitry, and a PIA Input/Output Interface.

The video tape did not fully discuss the operation of each circuit, but covered only those aspects that may have an impact on servicing.

The tape began with the operation of the memory circuitry. This consists of twelve ROMs: IC1 through IC12. To show how this circuit works, the video first examined the memory scheme.

Defender’s main program requires that there be 4k of memory present in or between ROMs or pairs of ROMs. These include: IC1 and 4, IC2 and IC3. These ICs contain memory for addresses D, E, and F000.

In certain versions of Defender, some of the ROMs are only 2k memory devices. In these versions, the memory circuitry operates slightly different than the 4k memories. It is important to recognize this when troubleshooting the ROM board.

The memory pairs work like this. If IC1 is a 2k memory device, then IC4 must also be a 2k memory device in order to provide the necessary 4k of memory required by the system program.

When the memory is split in this manner, the upper/lower ROM decoder Lower-half-enable-not signal is connected to pin 18 of IC1, and the upper/lower ROM decoder upper-half-enable-not signal is connected to pin 18 of IC4. These signals select memory section halves D000 or D800.

While the memory section half is being selected, the ROM/Page decoder selects the memory section by supplying a signal to pin 20 of each of the memory pair ICs.

Note that jumpers W2 and W4 must be in place when the ICs are 2k memory devices. These jumpers are needed to make the pin 20 connection common to both IC's and to connect the UE signal to IC4.

Pin 18 of IC1 is address bit All and pin 18 of IC4 becomes the input for the PLE signal through jumper W3 from the upper/lower ROM decoder. IC2 and IC3 are 4k devices. IC6 is used to hold extra game features.

Each of the ROM ICs perform the following functions... ICs 1, 2, 3, and 4 contain general game programs… In addition IC3 provides power-up scan tests… IC5 is not used… IC6 provides hyper-space activities... ICs 7 and 10 contain system diagnostics... ICs 8 and 11 provide all text information that appears on the screen… and ICs 9 and 12 operate the attract mode and contain the high-score-to-date information.

The next ROM board circuit the video covered was the page select decoder. This circuit provides page-enable signals PS0 through PS9 using MPU data bits.

These data bits are BCD input signals to IC17, which when clocked, presents these bits to pins 15, 14, 13, and 12 of binary-to-decimal converter IC13.

This occurs whenever the E clock, read/write input from the MPU address bus, and the memory section D enable signal all go low. IC13 then provides an enable signal to one of ten possible pages. These are determined by the BCD input from the MPU data bus.

Memory selections sections C, D, E, and F000, are made by IC15 and MPU address bits A15, A14, A13, and A12. Address bits A12 and 13 provide the selection input, and bits A14 and 15 provide an enable clock pulse from pin 8 of IC18.

When page zero is selected by IC13 (PS0), and memory section C is selected by IC15 (PE), pin 3 of IC14 goes low, effectively producing the PE/PS0 for input to the page zero decoder on the CPU/Video board.

The next ROM board circuit covered was the ROM Section/Half Decoder. This decoder uses MPU address bit All and the MPU read/write signal to determine the memory section half (or 2k memory block) addresses by the main program read/write signal to determine the memory block) addresses by the main program.

When address bit All is low, IC19 presents a high to pin 5 of IC18. When the read/write signal is high, the output of IC18 (pin 6) is low, enabling the lower half of the selected main memory section.

When address bit All is high and the MPU read/write signal is high, pin 3 of IC18 is low, enabling the upper half of the selected main memory section.

The final circuit that the video covered was the PIA and its associated decoder. The PIA decoder uses inputs from the MPU address bus and the section/page decoder. Address bits A10 and 11 are applied to pins 14 and 13 of IC15. A low output at pin 9 is produced when A10 and All are both high and the page-enable-not signal from the section/page decoder is low. This output is then gated with MPU address bit A4 and the page-select-zero-not signal from the section/page decoder to produce ROM PIA address CC10.

On the PIA itself data bits zero through 7 from the MPU data bus are used for inputs and outputs to and from the coin door switches and sound module.

Inputs CA1, CA2, and CB1 are from the count 240 circuit, the coin door slam switch, and function VAll from the video address generator. The negative-to-positive transition of any of these inputs cause Interrupt-request-not to go low. The MPU then reads the PIA to determine which input occurred.

MPU address bits A0 and A1 are applied to pins 35 and 36 of the PIA for register select zero and register select one controls. The read/write signal from the MPU is applied to pin 21 and controls the direction of data flow through the PIA.

The E input at pin 25 is the clock source for the PIA. The reset circuit input to the PIA at pin 34 is used to clear the PIA registers when the game is being reset.

As can be seen the ROM board is highly interactive with the rest of the circuitry in Defender.

It is important to take this into consideration when troubleshooting or servicing the ROM board. The video tape assumed that you have isolated any problems to the ROM board and therefore covered only the ROM board itself.

The video tape began the troubleshooting section as in all troubleshooting procedures, by recommending that you check the supply voltages to the board. ROMs are very sensitive to their operating voltages and a low regulated 5 volts will cause the ROMs to malfunction, even though there is nothing wrong with the ROMS themselves.

Once you are satisfied that the operating voltages are proper, check the connectors and cables to the board. A loose or faulty cable can also cause the ROMs to appear to be bad. Once you have determined that the power supply voltages and connectors to the board are okay, you may want to swap-out the ROM board. Doing this will enable you to positively determine that the ROM board is at fault before spending a great deal of time troubleshooting the board.

Begin actual troubleshooting of the ROM board by running a system start-up test. Upon turning the system on, you will see a variegated screen scanned twice. The system will then self-test and display a message indicating if there is a malfunction.

If you get a failure at this point, perform the ROM test that is included in the self-diagnostics. This test will indicate specifically, which ROM is bad.

If the self-diagnostics ROM test will not run, insert a known good IC3 and run the power-up test again.

During this procedure, if IC 7, 8, 10, or 11 is bad, the screen will show continuous variegated scans.

If IC 1, 2, 4, 6, 9, or 12 is bad, the screen will display an error message.

If this ROM test produces no results, it can be assumed that the ROMs are okay. The next step is to check out the remainder of the circuitry on the ROM board. Since the ROM board functions through control signals generated throughout the system, this can be a difficult task.

One way to make this easier is by using a no-op socket. This is a specially built socket that replaces the MPU IC on the CPU/Video board. The no-op socket causes the MPU circuit to act like a counter, generating a continuous series of clock pulses which can be likened to address bits.

Now, with the MPU generating continuous address bits, the remainder of the ROM board can be checked using a logic probe. By following the schematic diagram and probing the various IC's, it can be determined if an IC is responding appropriately to the MPU generated address bits.

This is the only sure and convenient way of checking out the soldered ICs on the ROM board. If you are going to be troubleshooting the ROM boards and not just swapping them out, it is recommended that you contact Williams Electronics service representatives about the no-op socket.

When checking out the ROM board, remember that certain versions of Defender use 2k ROMs which require the use of jumpers. Be sure and check your schematic to determine if these jumpers are being correctly used when required.

This concluded the video tape.