CPU BOARD

Part 2
CPU Oscilloscope Troubleshooting

SERVICING SERIES

Williams® ELECTRONICS, INC.

CPU OSCILLOSCOPE TROUBLESHOOTING

Welcome to Williams Electronics video-based servicing series. This Recap Sheet contains the most important points covered in the accompanying video tape. Use the recap sheet to assist you later on in recalling information as you need it while troubleshooting. This recap covers troubleshooting the CPU board for the Defender Game, using a multimeter, a logic probe, and an oscilloscope.

Also included with the recap sheet are a series of checkpoint charts showing the test points at which you should take 'scope' readings, and what you should see. These scope readings and some common timing considerations are discussed in this recap. All of the oscilloscope timing measurements depicted in the video tape are provided here for your reference during actual servicing situations. You will have to use your schematic diagrams in conjunction with the recap information.

Since the information contained here is a continuation of the troubleshooting begun in tape one, it is assumed that you have completed certain checks and replaced some of the board chips before beginning the procedures covered in the second tape. Here are the things that should be done before starting oscilloscope troubleshooting.

CHECK CMOS RAM POWER SUPPLY

First, check the battery voltage in the on-board CMOS RAM power supply, with the Defender main power off. This should be about 4 volts at the cathode of diode D14. Also check the condition of diodes D13 and D14.

Next, check that all connectors are tight and that all socketed parts are secure in their sockets. It is a good idea to remove and replace all ribbon connector plugs to be sure that they are completely seated.

CHECK DC VOLTAGES ON POWER BUSSES

The next step is to power up Defender and check the DC voltages on the power busses. Remember that logic circuits, especially ROMS, are very sensitive to low voltages. A perfectly good part can appear to be defective with a slight voltage drop.

After you are sure that the main power busses are at the correct level, complete the steps in the troubleshooting flow chart, using a logic probe. (See the recap sheet for tape one of the CPU servicing.)

As you work through the steps of the troubleshooting flow chart, you will replace certain socketed parts. The parts include the MPU . . . The Vertical and Horizontal Decoder ROMS . . . and the twenty-four chips in the Video RAM Banks . . . For most steps on the flow chart, you will check the pulsing at one or more chip pins. On the Reset, Watchdog and Screen Control Circuits, you will check for a constant high or low level.

If you fail to find pulsing, or if you find pulsing where a constant level is expected (or any other inconsistency), isolate and repair the problem. Once you locate a problem, repair it and then retest the circuit.

Having completed these tests and replaced the parts indicated, if you still have not found the fault, the chances are good that it is a timing problem. While timing problems are rare, they can occur, and you will need an oscilloscope to track them down. This tape discusses where to look with the scope, and what you should see.

CHECK WATCHDOG CIRCUIT

First check the Watchdog circuit. The Watchdog circuit is a timer which resets the MPU every 133 milliseconds if it is not cleared by the game program. Check the output of the Watchdog at pin 13 of chip 5M.

You should see a high level and no pulsing in a properly operating circuit. This indicates that the game program is clearing the Watchdog before it can reset the MPU.

If you see a trace which is 266 milliseconds between the leading edges of successive pulses, the most likely cause is an MPU lockup.

If you see a trace which consists of a pulse 133 milliseconds long, followed by a second pulse of 133 microseconds, then the cause is most likely a defective MPU, a bad ROM, or a faulty Color RAM.

Another possibility is a defective chip in the Watchdog circuit. To determine if the problem is in the Watchdog circuit, cut the pad connecting the 5M OR

Gate to the 5O (5 "OH") Timer.

If you cut the pad and it cures the problem, stopping the incorrect pulsing at the Watchdog output and cleaning up the video, then you should look for the fault in the Watchdog Circuit.

If the fault is not in the Watchdog, you will usually get one or two "Carpet Pattern" screen scans on newer boards, then a screen crash. In that case, re-solder the pad of the Watchdog, and continue troubleshooting. You should suspect a faulty MPU, a problem in the ROM Board, or a problem in a CPU component which must read data buss information.

Once you have determined that the problem is not in the Watchdog Circuit, the next point to check with the scope is the clock outputs of chips 6R and 7P.

The timing signals to look for are shown on the appropriate timing charts. The basic clock frequency is a 12 Megahertz pulse at pin 8 of chip 7P. This signal also appears as an inverted 12 Megahertz pulse at pin 10 of 7P. If you don't see the 12 Megahertz output of 7P, then the problem is most likely the 7P chip or the crystal.

The next check point is pin 3 of chip 7R, here you should see an asymetrical 4 Megahertz output. At pin 6 of the same chip, you should see an inverted version of the same signal.

Finally, you should see symmetrical 4 Megahertz, and inverted 4 Megahertz outputs at pins 9 and 8 of chip 6R, and a 6 Megahertz output at pin 6 of 6R.

CHECK E AND Q GENERATOR CIRCUIT

The next check after the Clock Circuit is the E and Q Generator Circuit. The E and Q Generator provides overlapping clock signals necessary to the operation of the MPU, Video RAM Timing and several other circuits.

You should see a symmetrical input pulse with an interval of 500 nanoseconds between the trailing edge of one pulse and the trailing edge of the next, at pin 5 of chip 7J.

You should also see a symmetrical "E" output pulse with an interval of one microsecond between the trailing edges of two pulses, at pin 9 of chip 7L.

If you have a dual trace scope, you should also see that the leading edge of the "Q" output (pin 5 of chip 7L) leads the leading edge of the "E" output by 250 nanoseconds. Any variations from these timings will prevent proper game operation.

CHECK VIDEO ADDRESS GENERATOR CIRCUIT

With proper output from both the Clock and E and Q Generator circuits, the next check is the Video Address Generator Circuit. The Video Address Generator supplies the address bits which scan the Video RAM.

Given correct DC voltage on the 5 volt buss, 4 Megahertz in from the Clock, and no reset signal, the Video Address Generator should have the timing outputs shown in the appropriate timing chart.

If the timing is not as shown, start troubleshooting at the 5J counter, then go to 5H, 5F, 5E and the remaining components. Once the Video Address Generator is known to be good, move on to the Video RAM Control Circuit. The Video RAM Control allows the MPU to sequentially address the Video RAM Banks.

You should see a timing pattern on the Video RAM Control MUX 1 line at pin 12 of chip 6P. You should also see Enable pulses at pins 3 and 11 of chip 5P, and pin 6 of chip 4R. Write pulses should appear at pins 3, 8 and 11 of chip 4R. If the timing is not as shown, check out the circuit.

CHECK VIDEO RAM TIMING CIRCUIT

The next checkpoint is the Video RAM Timing Circuit. This circuit uses the 12 Megahertz and E and Q outputs to produce timing pulses required for access to the video RAM. You should see outputs on the 5S, 6P and 4J chips. In case of problems, check the 4S data latches first, and then the remainder of the circuit.

CHECK MONITOR SYNC GENERATOR CIRCUIT

The Monitor Sync Generator Circuit is the next circuit to check with the 'scope. The Monitor Sync Generator derives vertical and horizontal sync pulses for the Monitor by counting video addresses. Check for vertical and horizontal sync pulses at pins 8 and 11 of chip 3A.

The Address Bus brings Video Address information to the 3B, 4C and 5B chips. These chips decode the address count and selectively assert inputs to the

exclusive OR gates of chip 3A. When gated with ground, these inputs result in Vertical and Horizontal Sync Pulses and a Composite Pulse, which is not used in this game.

You should see a vertical sync pulse occurring every 16.6 milliseconds, with a 0.77 millisecond pulse width. The horizontal pulse occurs every 64 milliseconds and is 4 microseconds wide.

In addition to sync signals, blanking is needed for proper video operation. The Blanking Circuit decodes video address information and provides a blanking signal to the Video Driver Circuits whenever the scan passes screen limits. This additional memory area is used for MPU scratchpad, and the blanking signal prevents possible interference between scratchpad and normal video access.

Check for a blanking signal output on pin 8 of chip 4B.

As with the other circuits described in the video, you should check for any additional problems in the circuit.

CHECK COUNT 240 CIRCUIT

The final circuit to be considered is the Count 240 Circuit. This circuit provides an interrupt signal when the screen scan gets to the bottom of the screen at Count 240 (240 lines of video).

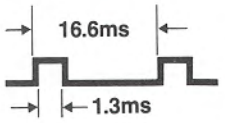
You should check for a Count 240 output at pin 8 of chip 4C.

The timing pattern on the Count 240 Circuit is a 1.3 millisecond pulse occurring each 16.6 milliseconds.

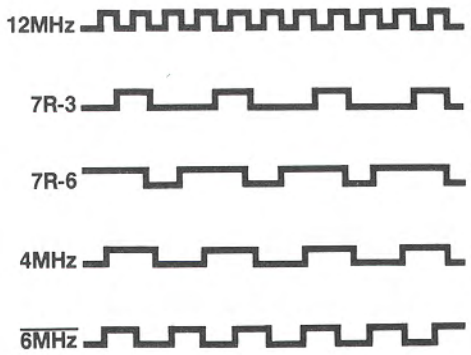
If you know that the Video Address input to the Count 240 circuit is good, but there is no pulsing at the output, replace the 4C chip.

This completes the two-part series on Defender CPU Video Board Servicing.

OSCILLOSCOPE TIMING CHARTS



(At Chip 4C, Pin 8)



(Output at Chip 7P, Pin 8)

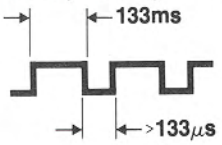
(Output at Chip 7R, Pin 3)

(Output at Chip 7R, Pin 6)

(Output at Chip 6R, Pin 9)

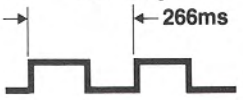
(Output at Chip 6R, Pin 6)

Indicates Faulty MPU, ROM, or RAM



(Faulty output at Chip 5M, Pin 13)

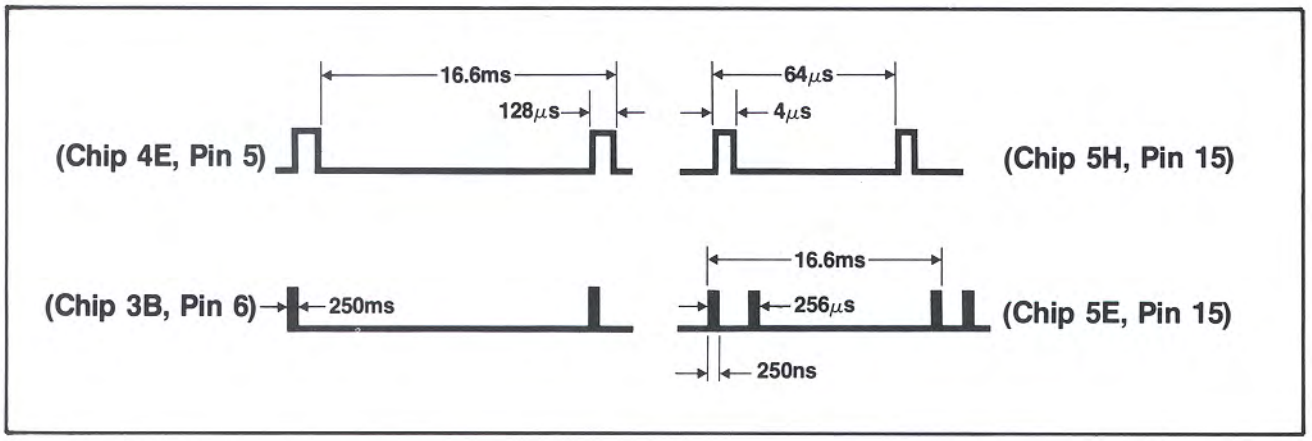
Indicates MPU Lockup

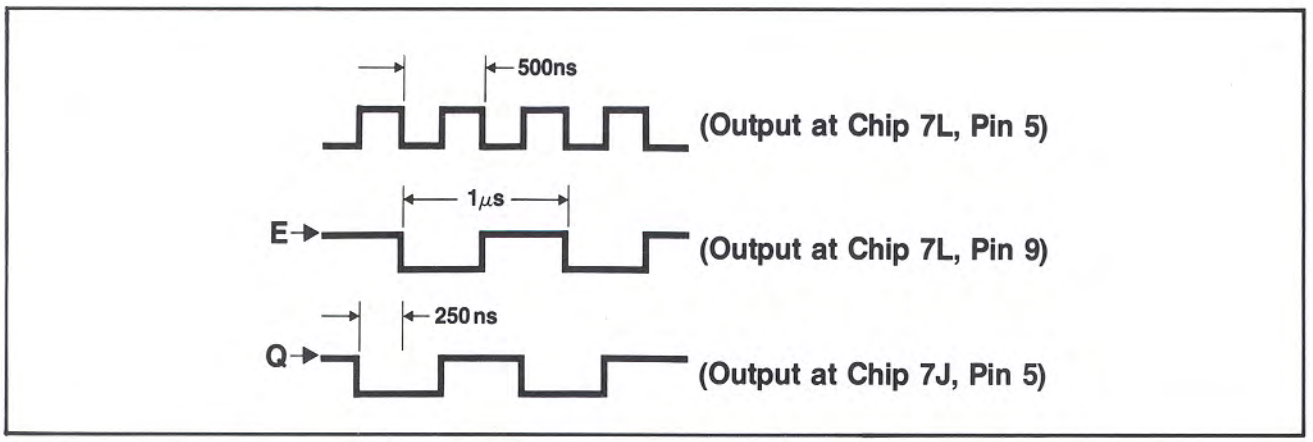


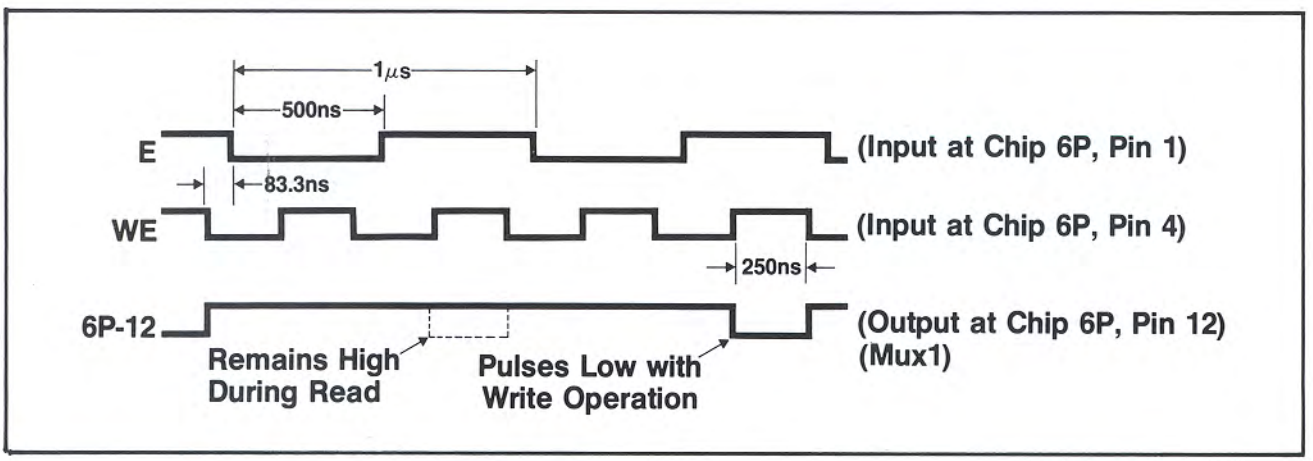
(Faulty output at Chip 5M, Pin 13)

*Note: Normal Output is high level constant signal.

OSCILLOSCOPE TIMING CHARTS

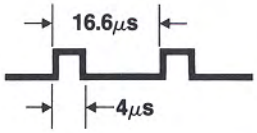




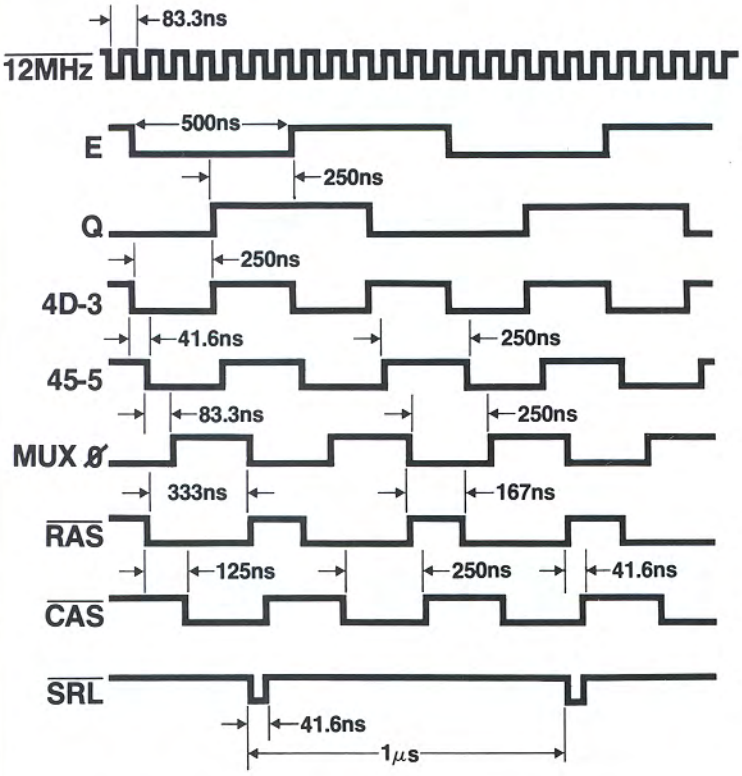


OSCILLOSCOPE TIMING CHARTS

(At Chip 3A, Pin 8)
(Vertical)



(At Chip 3A, Pin 11)
(Horizontal)



(Input at Chip 6M, Pin 9)

(Input at Chip 5R, Pin 5)

(Input at Chip 5R, Pin 4)

(Output of Chip 5R, Pin 3)

(Output of First Latch, 4S, Pin 5)

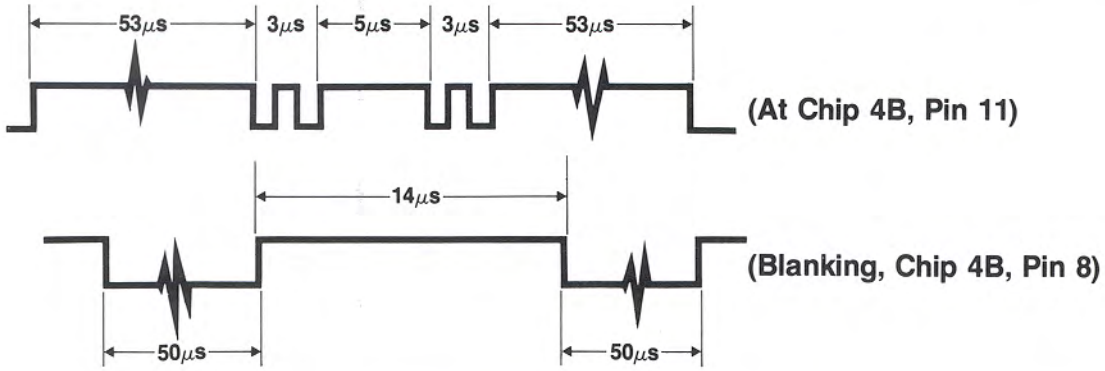
(Q Output of Second Latch, 4S, Pin 5)

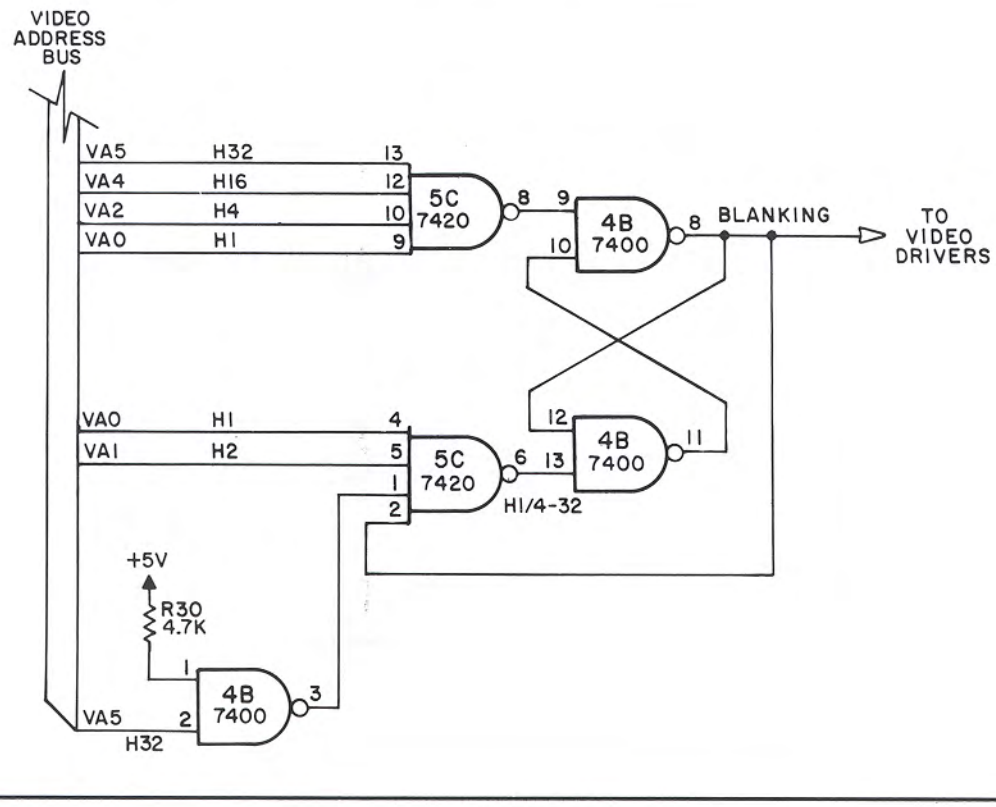
(Output at Chip 4J, Pin 9)

(Output at Chip 5S, Pin 5)

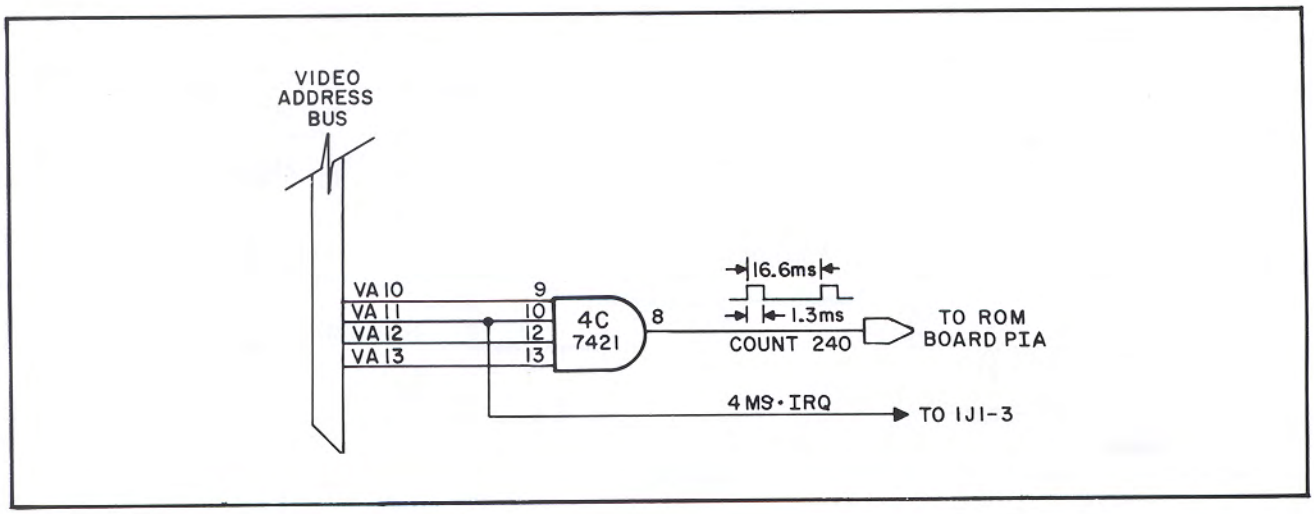
(Output at Chip 6P, Pin 8)

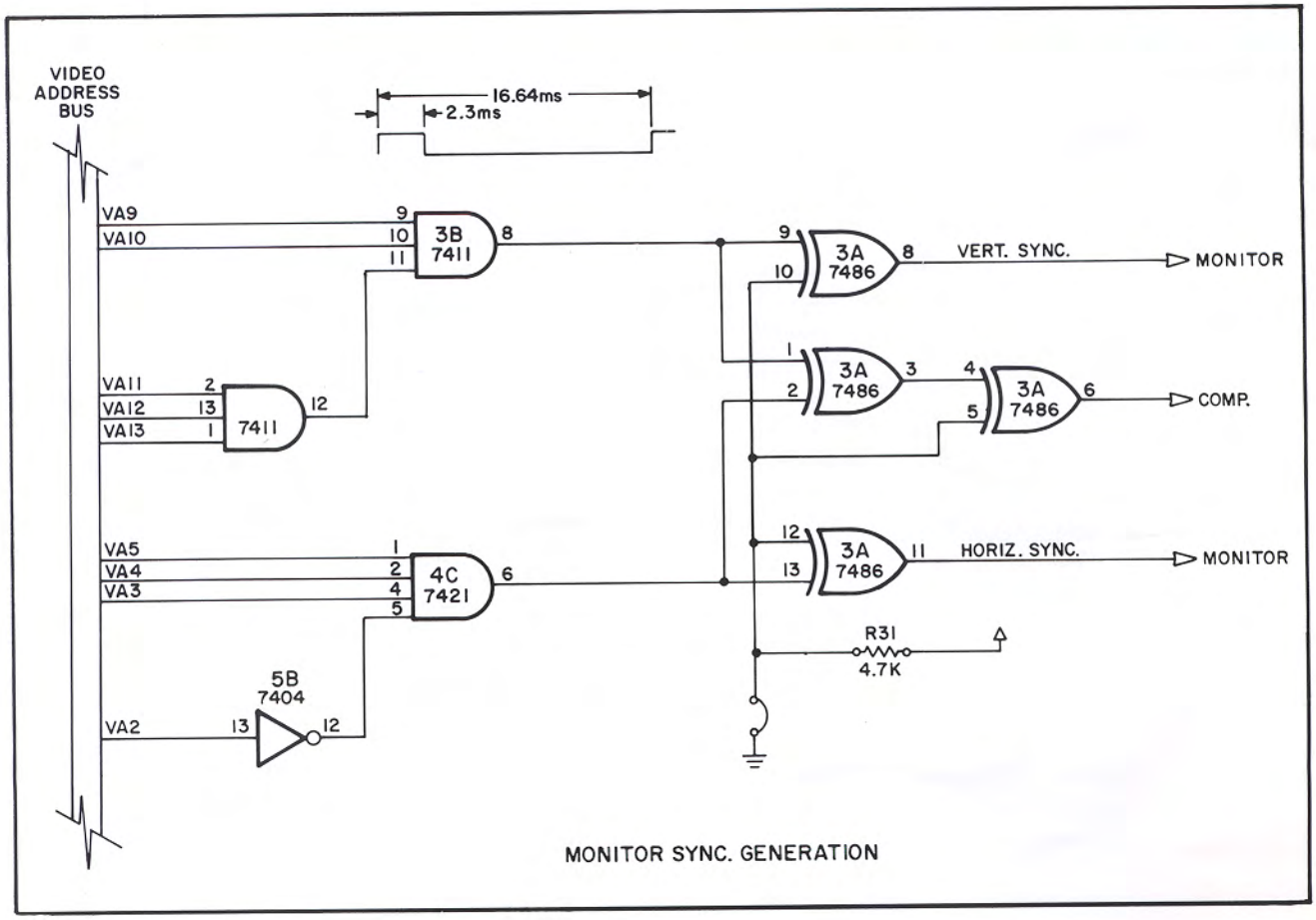
OSCILLOSCOPE TIMING CHARTS





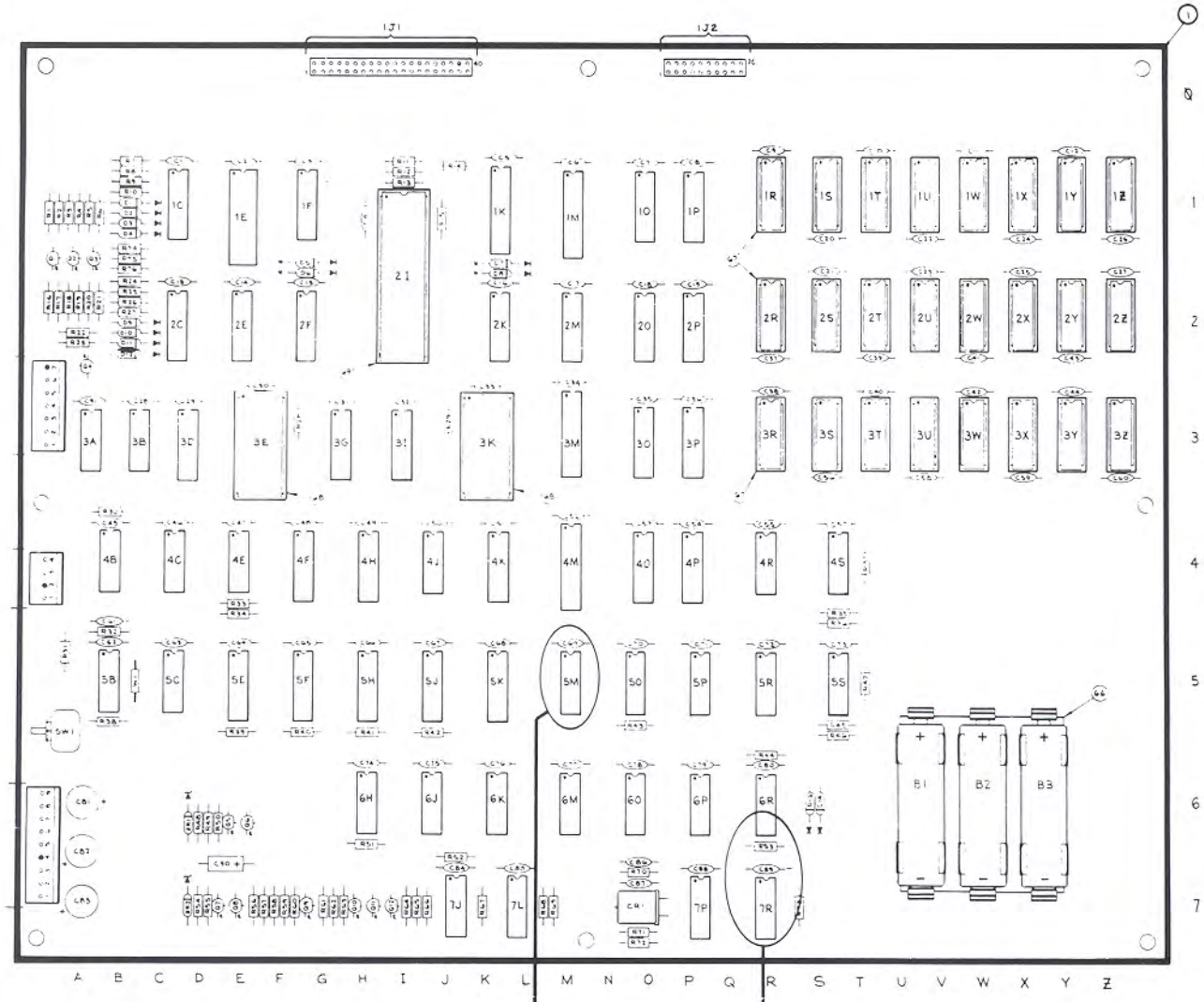
OSCILLOSCOPE TIMING CHARTS





MONITOR SYNC. GENERATION

OSCILLOSCOPE TIMING CHARTS



: Watchdog

Check For Output at Pin 14, 5M: High Constant, No Pulse

133ms / 133μs — Faulty MPU, ROM or RAM

266ms — Faulty MPU — Lockup

Checkpoint 2: Clock

Check For 4,6 and 12 Mhz at 6R and 7P Chips.

12MHz — (Output at Chip 7P, Pin 8)

7R-3 — (Output at Chip 7R, Pin 3)

7R-6 — (Output at Chip 7R, Pin 6)

4MHz — (Output at Chip 6R, Pin 9)

$\overline{6MHz}$ — (Output at Chip 6R, Pin 6)

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